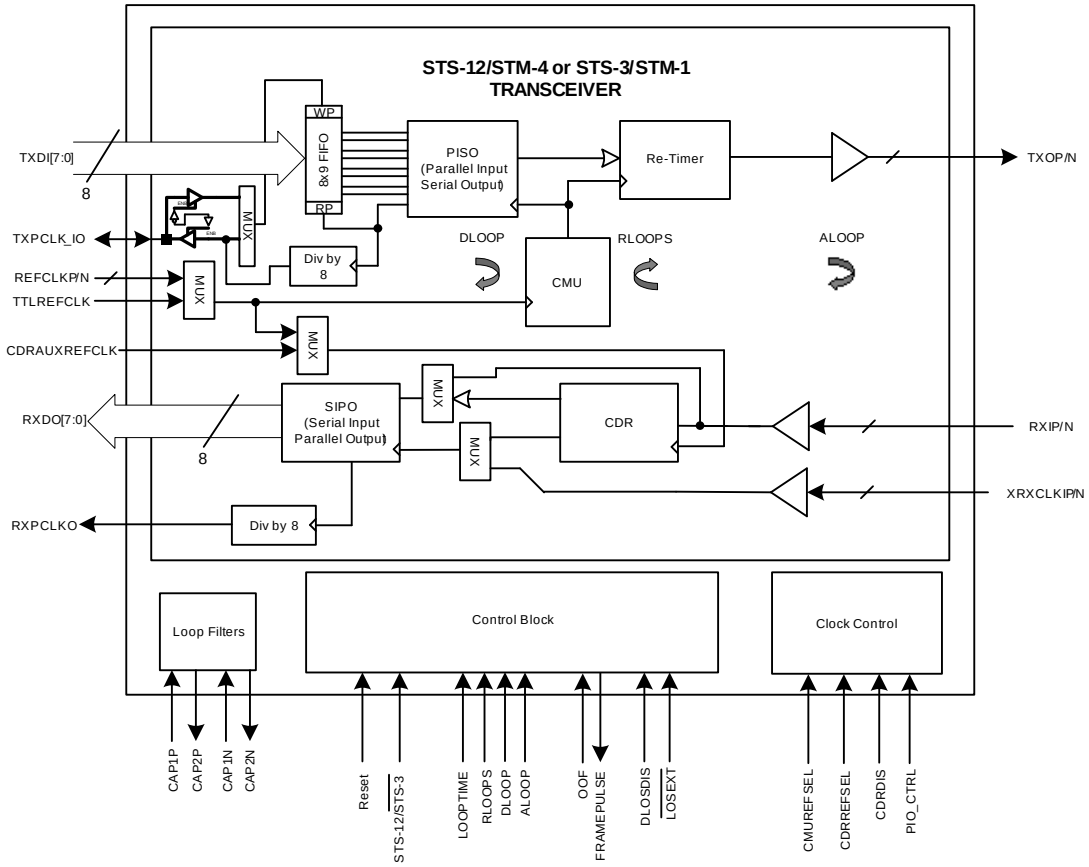
# 622.08/155.52 MBPS
# SONET STS-12/STS-3
# SDH STM-4/STM-1
# XRT91L30 Transceiver
# Evaluation Board User Manual

# SONET STS-12/STS-3 or SDH STM-4/STM-1
# XRT91L30 Optical Evaluation Board User Manual

Feb 09, 2006

**Figure 1.0 XRT91L30 Block Diagram**




## 1.0 OVERVIEW

This is evaluation board manual is intended to help the user become familiarized to operate the XRT91L30 Demo board and run traffic with minimum effort.

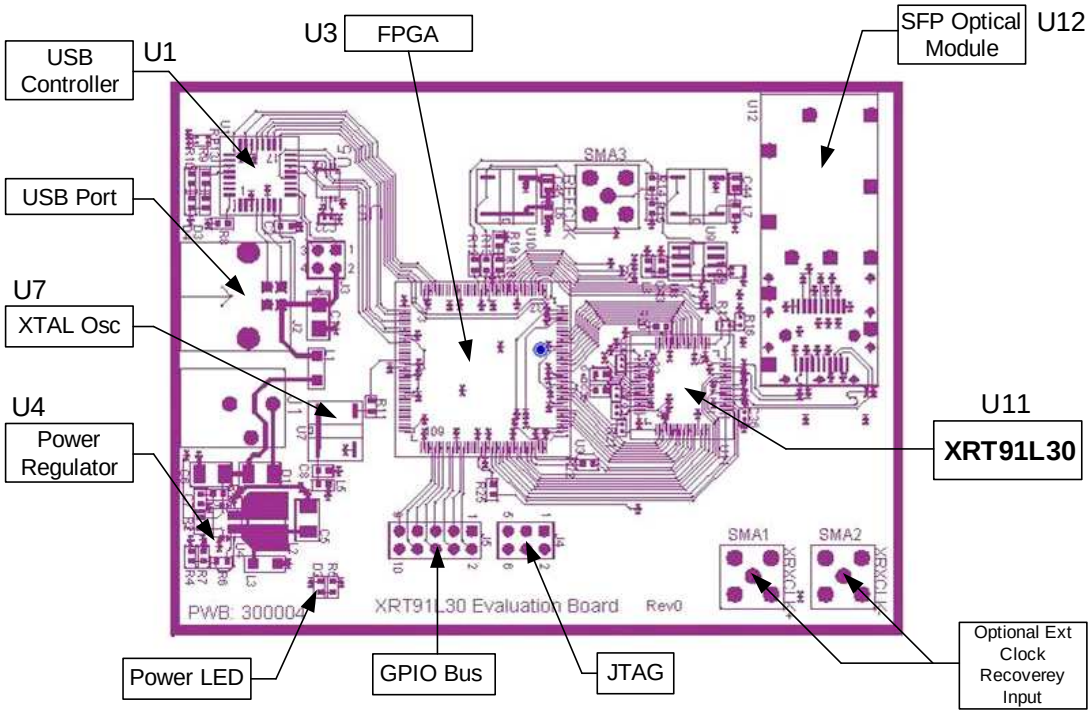
Requirements:

1. XRT91L30 Evaluation Board
2. OC-12/OC-3 or STM-4/STM-1 generator/analyzer test equipment with optical interface
3. A Windows PC with USB port & USB cable for power supply and GUI interface
4. XRT91L30 supplied USB drivers and GUI to be installed on the PC (using Win98, 2000, or XP)
5. XRT91L30 data sheet (rev P1.0.8 or newer)

## 2.0 EVALUATION BOARD ARCHITECTURE

XRT91L30 Evaluation board provides a simple and efficient way to quickly evaluate functionality and performance of the XRT91L30 SONET/SDH STS-12/STM-4 or STS-3/STM-1 Transceiver.

**Figure 2.0 XRT91L30 Optical Evaluation Board revision 0**




Evaluation board consists of XRT91L30 device (U11) connected to a Small Form Factor Pluggable (SFP) module (U12). Since the **XRT91L30 is a pure hardware pin control device and does not support microprocessor interface**, the XRT91L30 hardware control pins are interfaced to a field programmable logic device (FPGA) (U3). The logical level of the XRT91L30 control pins is controlled from a **G**raphical **U**ser **I**nterface (GUI) program installed on a personal computer (PC). Evaluation board power and GUI communication interface are then both provided through the **U**niversal **S**erial **B**us (USB) from the PC.

Other system level components on the evaluation board include a USB microcontroller (U1), a switching power regulator (U4) and a 77.76 MHz crystal oscillator (U7). There are several other optional components for evaluation of supported special features of the XRT91L30 device.

### 2.1 FPGA FUNCTIONALITY AND CONTROL

The FPGA controls most of the function of the device under test (DUT), in this case the XRT91L30. All access to XRT91L30 control pins are defined through the use of the Exar supplied XRT91L30 GUI.

### 2.2 XRT91L30 CLOCK REFERENCE

The 77.76 MHz oscillator clock is internally divided by four within the FPGA to generate19.44 MHz clock. The appropriate reference clock frequency is then selected based upon the polarity of CMUFREQSEL setting on the GUI. RefClk (TTL) FPGA output is then applied to the XRT91L30 TTLREFCLK input that feeds the **C**lock **M**ultiplier **U**nit (CMU) **P**hase-**L**ocked **L**oop (PLL).

A 77.76 MHz clock is also applied to the CDRAUXREFCLK input. CDRREFSEL setting will then determine the source of the **C**lock and **D**ata **R**ecovery (CDR) reference clock.

Differential reference clock input is not used on the evaluation board. However, it is possible to apply differential reference clock by installing some of the optional components. See evaluation board schematic for reference.

### 2.3 FPGA FEATURES

STS-12/STM-4 or STS-3/STM-1 optical signal is received by the optical module and converted to LVPECL electrical signal before being interfaced to the XRT91L30. The XRT91L30 then recovers the clock and data and converts the serial data to SONET/SDH byte wide parallel data and outputs the recovered divide-by-eight clock that is synchronous to the parallel data. The FPGA performs the task of the terminal end unit and allows a system level FPGA Remote Loopback function, where the received byte wide data coming from the XRT91L30 is looped back within the FPGA and sent to the byte wide transmit input interface of the XRT91L30.

**Note:**
This is system level loopback is significantly different from the XRT91L30 device's diagnostic Serial Remote Loopback. Serial Remote Loopback occurs internally within the XRT91L30 and received serial data is looped back to the transmitter before **ser**ial-**des**erializer (SERDES) conversion. Serial Remote Loopback is meant to be used for diagnostics.

In addition, the FPGA also contains a $2^{31} – 1$ PRBS pattern generator and PRBS data integrity checker. A status LED indicator called **Pattern Sync** indicates when the PRBS pattern is currently locked. Another status LED indicator called **Pattern Sync History** indicates if there was a momentary loss of PRBS sequence.

It is also possible to transmit a fixed pattern rather than PRBS by selecting the **32-bit User Pattern** and entering the fixed pattern on the **32-bit User Pattern window**. However, error checking is not performed when fixed pattern is being transmitted.

## 2.4 EVALUATION BOARD LIMITATIONS

1. ALOOP and DLOOP not supported when operating at STS-12/STM-4 rate using 19.44 MHz reference clock.
2. Transmit Parallel Clock must be configured for **Output** when transmitting $2^{31}$ – 1 PRBS pattern or 32-bit User Pattern.
3. Looptiming must be implemented when using FPGA Remote Loopback.

**Limitation 1:** Due to FPGA design limitations, the Evaluation Board currently does not support Analog and Digital Local Loopbacks in STS-12/STM-4 data rate mode using 19.44 MHz reference clock. This limitation will be removed in the future. At this time, one can use 77.76 MHz reference clock in STS-12/STM-4 data rates to invoke Analog and Digital Local Loopbacks. This limitation does not apply to STS-3/STM-1 data rates.

**Limitation 2:** The PRBS state machine design implemented the Transmit Parallel Clock Output (TXPCLK_IO) pin to be configured for **Output**. Therefore, set the **Tx P Clock Direction** to **Output** whenever transmitting PRBS pattern. This limitation also applies when using the 32-bit User Pattern generator.

**Limitation 3:** Whenever **FPGA Remote Loopback** is used, **Looptiming** must be implemented. This guarantees that transmit timing is synchronous to the signal source timing, thereby preserving data integrity at high SONET/SDH bit rates.

## 3.0 USB DRIVER AND GRAPHICAL USER INTERFACE INSTALLATION

This section details the installation of the software GUI provided as part of the evaluation process. It includes the following topics:



### 3.1 INSTALLING THE EXAR USB DRIVER

In order to operate the XRT91L30 GUI with the XRT91L30 Evaluation board, it is necessary to install the Exar USB drivers. Upon plugging the evaluation board into the computer, the system should recognize a new device and prompt for a driver. A window should appear similar to the one below.

**Figure 3.1 Add New Hardware**

The drivers are included in the Exar CD in the folder labeled Drivers. To install from the CD, select **Display a lists of all the drivers in a specific location, so you can select the driver you want**.

**Figure 3.2 Select Display Available Drivers and then Next**


**Figure 3.3 Select "Other detected devices" and then Next**

**Figure 3.4 Select Have Disk**

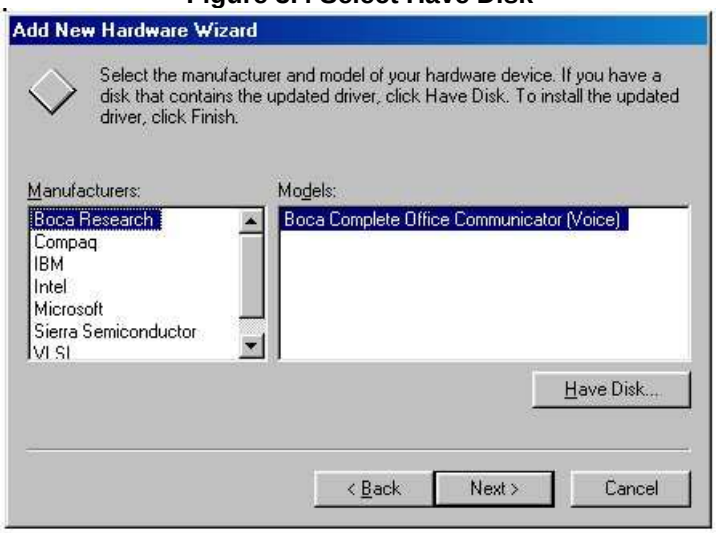
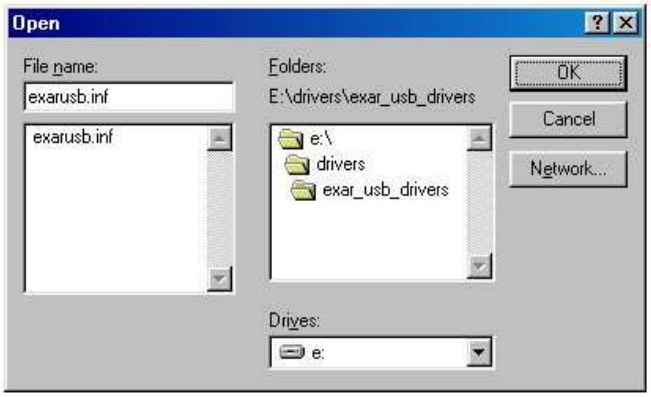
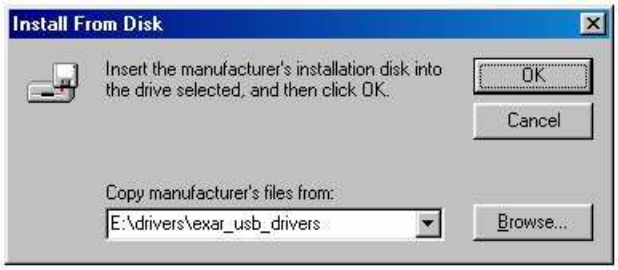



**Figure 3.5 Find the location of the drivers located on the CD**




The following window will appear confirming the location of the driver.
Select OK

**Figure 3.6 Install From Disk**



The driver will appear in the Have Disk window and should be selected. Press Next to install the driver.

**Figure 3.7 Driver Select**


Now that the system has found the appropriate drivers, select Next to install the Exar driver.

**Figure 3.8 Install Driver**

The driver is now installed in the system, and is ready to run the Exar Evaluation GUI.

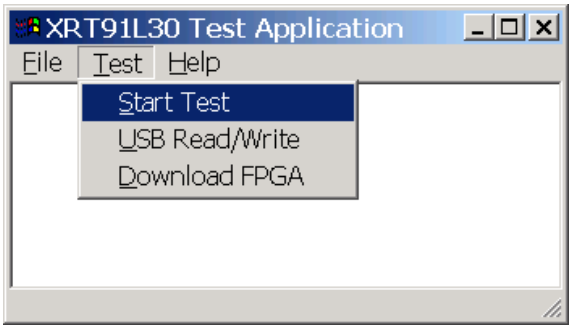
**Figure 3.9 Installation Successful**


**Note:**
Included in the driver zip package are two files: “exarusb.inf” and “exarusb.sys.” Upon first connecting the board to your computer, you may be prompted to install the Exar USB drivers. To install the drivers, follow the prompts and manually select the “exarusb.inf” file from the included driver zip file.

### 3.2 INSTALLING THE XRT91L30 EVALUATION GUI

To install the XRT91L30 GUI, double click on the installation file enclosed in the Exar CD, as part of the evaluation package. This will place the relevant GUI files in an Exar created folder along with the necessary FPGA file. Since the XRT91L30 is a pure hardware control device, it is necessary to drive the GUI through use of an FPGA file. This is automatically done when **Test->Start Test** is selected.

**Figure 3.10 Start Test**



## 4.0 XRT91L30 EVALUATION SOFTWARE

This section details the operation of the software GUI provided as part of the evaluation process. It includes the following topics:



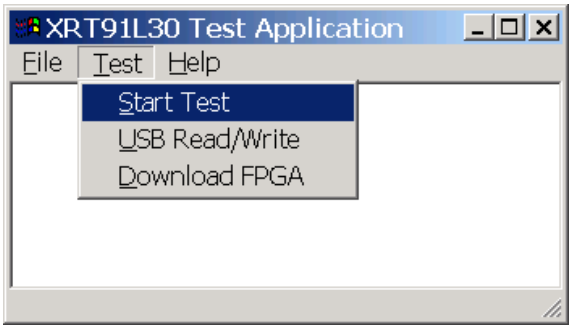
### 4.1 STARTING THE EVALUATION SOFTWARE

The evaluation software allows the user to do the following:

- Configure the XRT91L30 for proper operation
- Poll FPGA current PRBS Pattern Sync/History status
- Download a new FPGA code
- Enable/Disable XRT91L30 features with the click of a button

Once the XRT91L30 GUI is installed, it can be found through the **Start Menu->Exar->XRT91L30 Evaluation**. Once selected, it will open up the application. To begin the GUI, select **Test** from the menu bar and then **Start Test**. The GUI will automatically download the FPGA before it starts. To download a different FPGA than the default offering, select **Test->Download FPGA**.

**Figure 4.1 Start Test**



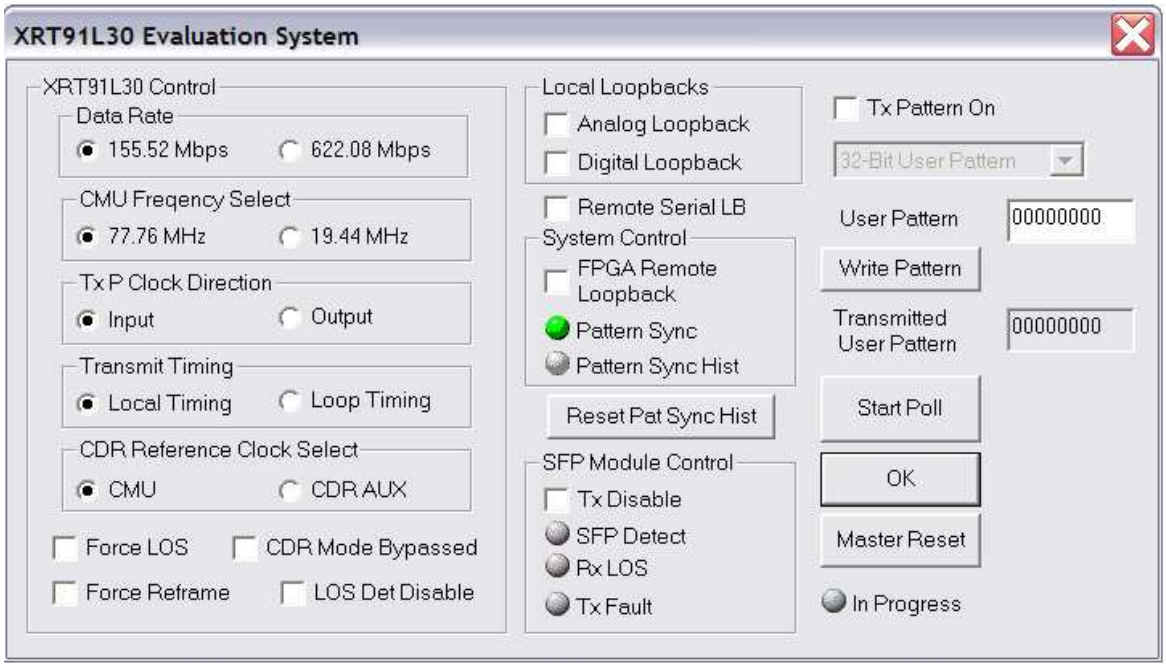
### 4.2 USING THE EVALUATION SOFTWARE

It is possible to achieve full device functionality through the GUI. Selecting a check box will enable/disable a certain feature. Upon each selection, the control pin assertion occurs immediately and is displayed in the main GUI window. In addition, FPGA features are also accessed and can be enabled or disabled through the main GUI window.

Status indicators will begin polling upon selecting the **Start Poll** button and will continue to poll every 250 milliseconds until it is stopped. Upon polling, the value of the transmitted pattern will be displayed in the transmit pattern section. To send a desired 32-bit sequential pattern, enter the relevant 4 byte value in the data box and select "**Write Pattern**." However, the **Tx Pattern On** needs to be enabled to begin transmission of selected pattern.

Clicking on **OK** will close the main window.

**Figure 4.2 Main GUI Window**



### 4.3 XRT91L30 GUI CONTROL DISPLAY ASSOCIATION

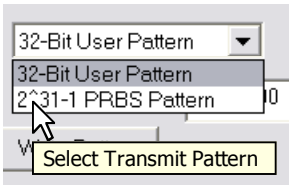
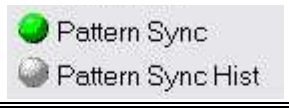
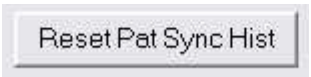
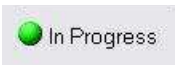
Below is a table outlining the GUI software control display association to the XRT91L30 hardware control pins.

**Table 1.0 XRT91L30 GUI Display Cross Reference**

| Main GUI Window Control Display | **XRT91L30** Hardware pin | Name | Hardware Pin description |
|---|---|---|---|
| Master Reset | 1 | RESET | Master Reset |
| Data Rate: 155.52 Mbps / 622.08 Mbps | 59 | STS-12/*STS-3 | Data Rate Selection |
| CMU Freqency Select: 77.76 MHz / 19.44 MHz | 3 | CMUFREQSEL | Clock Multiplier Unit Reference Frequency Select |
| Tx P Clock Direction: Input / Output | 48 | *PIO_CTRL | Transmit Parallel Clock Input/Output Select |
| Transmit Timing: Local Timing / Loop Timing | 2 | LOOPTIMING | Looptiming Select |
| CDR Reference Clock Select: CMU / CDR AUX | 60 | CDRREFSEL | Clock and Data Recovery Reference Frequency Select |
| ☐ Force LOS | 33 | *LOSEXT | Signal Detect Input<br>☐ = Normal Mode<br>☑ = Force LOS/Data Mute |
| ☐ Force Reframe | 11 | OOF | Out of Frame Input Indicator<br>☐ = Normal Mode<br>☑ = Force Reframe |
| ☐ CDR Mode Bypassed | 12 | CDRDIS | Clock and Data Recovery Unit Disable and Bypass<br>☐ = Internal CDR Enabled<br>☑ = Internal CDR Bypassed |
| ☐ LOS Det Disable | 7 | DLOSDIS | Internal LOS Detect Disable<br>☐ = Monitor and Mute upon LOS<br>☑ = LOS detect disabled |
| ☐ Analog Loopback | 64 | ALOOP | Analog Local Loopback Enable<br>☐ = Normal Mode<br>☑ = ALOOP Enabled |
| ☐ Digital Loopback | 62 | DLOOP | Digital Local Loopback Enable<br>☐ = Normal Mode<br>☑ = DLOOP Enabled |
| ☐ Remote Serial LB | 63 | RLOOPS | Serial Remote Loopback Enable<br>☐ = Normal Mode<br>☑ = RLOOPS Enabled |

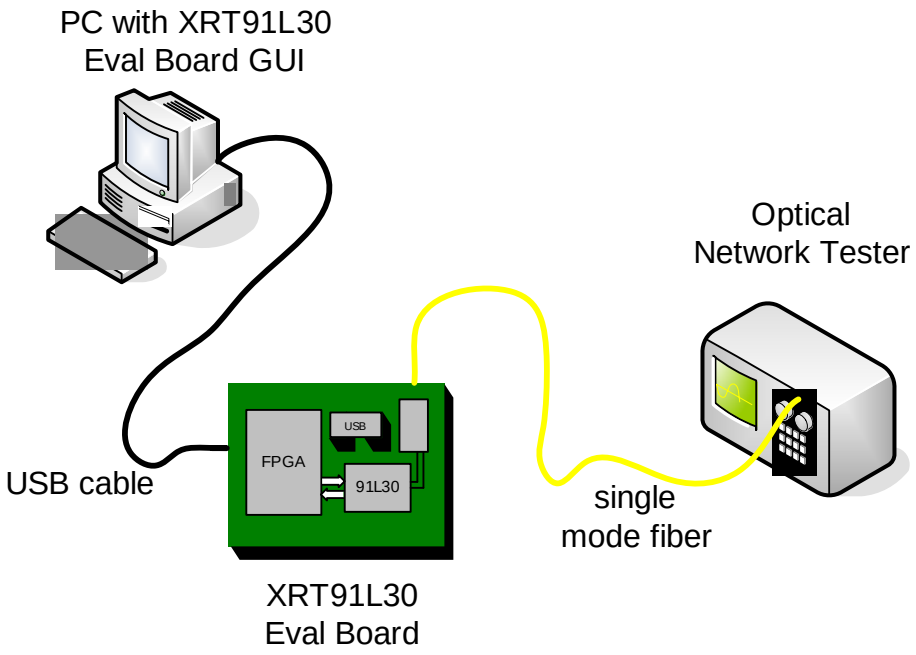
In addition, the table below also outlines the GUI control display association to the FPGA features and functions.

**Table 1.1 FPGA Functions GUI Display Cross Reference**

| Main GUI Window Control Display | FPGA Function | Functional Description |
|---|---|---|
|  | FPGA Remote Loopback | FPGA receives byte-wide parallel data/clock from RXDO[7:0]/RXPCLKO pins and loops data back to the TXDI[7:0]/TXPCLK_IO pins of the XRT91L30<br>☐ = Normal Mode/Thru Mode<br>☑ = FPGA Loopback Enabled |
|  | Tx Pattern On | Enables transmission of Selected Pattern<br>☐ = No transmit pattern selected<br>☑ = Begin pattern transmission |
|  | Pattern Select | Selects User desired 32-bit pattern or Auto-generated $2^{31}$ – 1 PRBS pattern |
|  | User Pattern | 32-bit User Pattern Hexadecimal Key Entry |
|  | Write Pattern | Writes desired pattern into buffer |
|  | Transmitted User Pattern | Indicates transmitted user pattern |
|  | Pattern Sync | Indicates PRBS pattern sync status |
| | Pattern Sync Hist | Indicates PRBS pattern error history |
|  | Reset Pattern Sync | Resets Pattern Sync History indicator |
|  | Polling in Progress | Indicates currently polling |

## 5.0 SETTING UP THE XRT91L30 EVALUATION BOARD FOR SONET/SDH TESTING

**Figure 5.1 Transceiver Test Setup**




Use the following steps in configuring the XRT91L30 Evaluation Board.

1. Install Exar supplied USB drivers and XRT91L30 GUI on the PC.
2. Connect the Exar supplied standard USB cable to the PC.
3. Connect PC USB cable to the USB Port on the board. Verify power supply on the board by checking Power LED.
4. Connect optical cable to SFP module.
5. Launch XRT91L30 GUI Application.
6. Configure the XRT91L30 for proper data rate and operation.

## 6.0 EXAMPLE APPLICATIONS

The following example applications are provided in this manual:



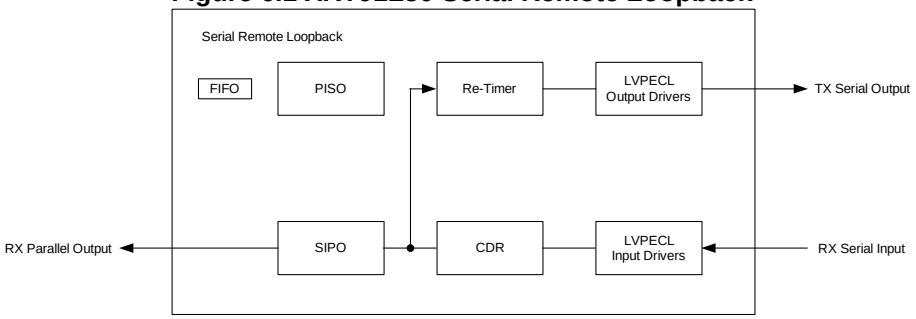
## 6.1 LOOPBACK OPERATIONS

Loopback operations generally fall under 2 different categories and are referenced with respect to the device. Remote loopback and Local Loopback are both available on the XRT91L30 device. Remote Loopback indicates that remote equipment (test equipment) signal is routed back to the equipment. Hence, all types of remote loopback routes received signal back to the transmit side. Local loopback indicates that link layer or terminal equipment signal (hence, local signal) is routed back to the link layer or terminal equipment. This means locally transmitted signal is routed back to the receiver.

### 6.1.1 Serial Remote Loopback

To quickly diagnose line integrity back to remote or test equipment, a serial remote loopback can be invoked.

**Figure 6.1 XRT91L30 Serial Remote Loopback**




**Configuring for Remote Serial Loopback Operation**

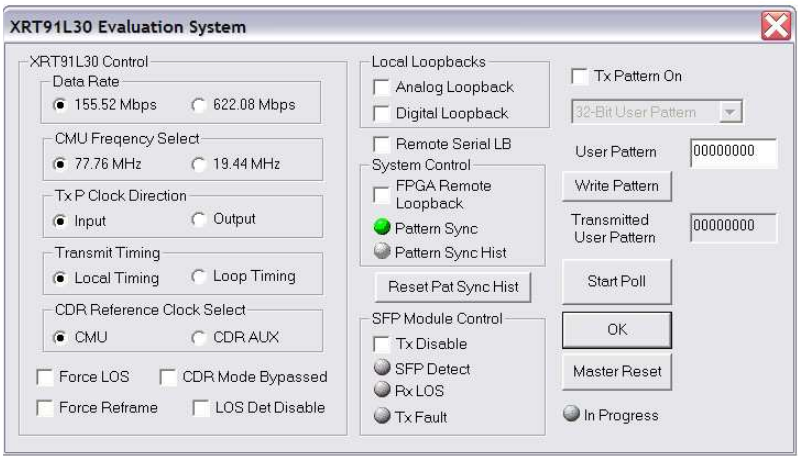
**Step 1.** With the Exar USB drivers and the XRT91L30 GUI installed, connect the USB cable to both the PC and the XRT91L30 Evaluation Board. Verify power supply on the board by checking Power LED.

**Step 2.** Connect the optical cable from the test equipment optical interface to the SFP optical module on the Evaluation Board. This cable is included in the XRT91L30 evaluation kit.

**Step 3.** Launch the XRT91L30 application GUI. See section 4.1, “Starting the Evaluation Software.”

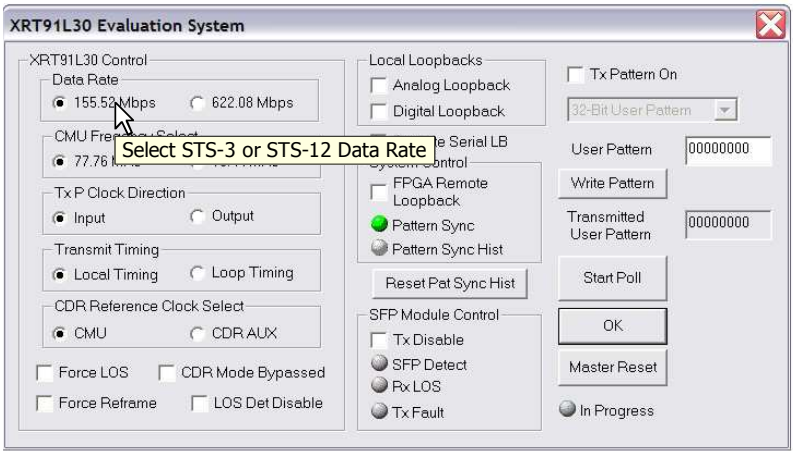
**Step 4.** Once the application GUI **Start Test** is running, you should see a similar window below with the XRT91L30 default settings.

**Figure 6.2 Main GUI Window**



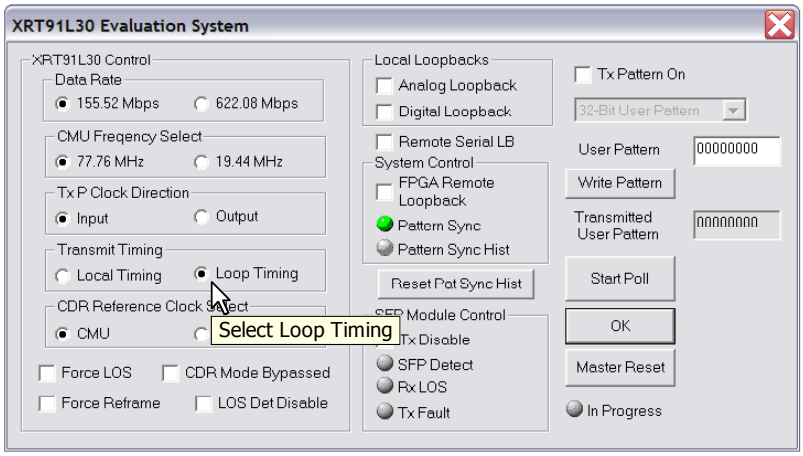

**Step 5.** Select the desired Data Rate signal:
STS-3/STM-1 at 155.52 Mbps or STS-12/STM-4 at 622.08 Mbps

**Figure 6.3 Select Data Rate**



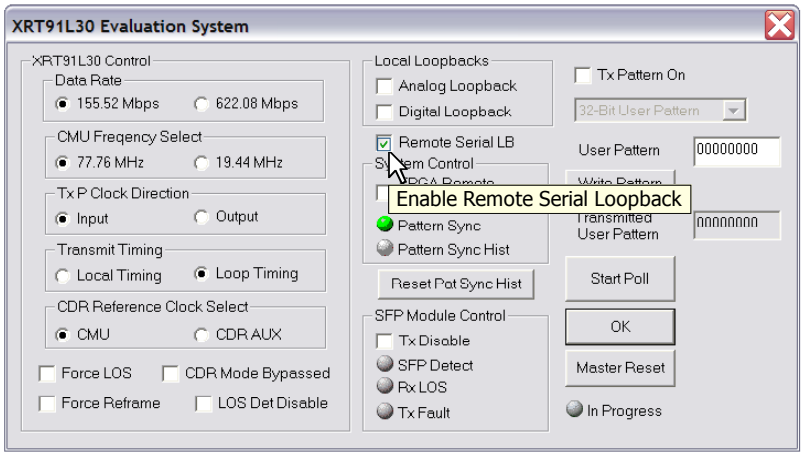
**Step 6.** Select **Looptiming** mode for the XRT91L30 transmit timing.

**Figure 6.4 Select Looptiming**




**Step 7.** Enable the Remote Serial Loopback by checking the on the “Remote Serial LB” box.

**Figure 6.5 Enable Serial Remote Loopback**

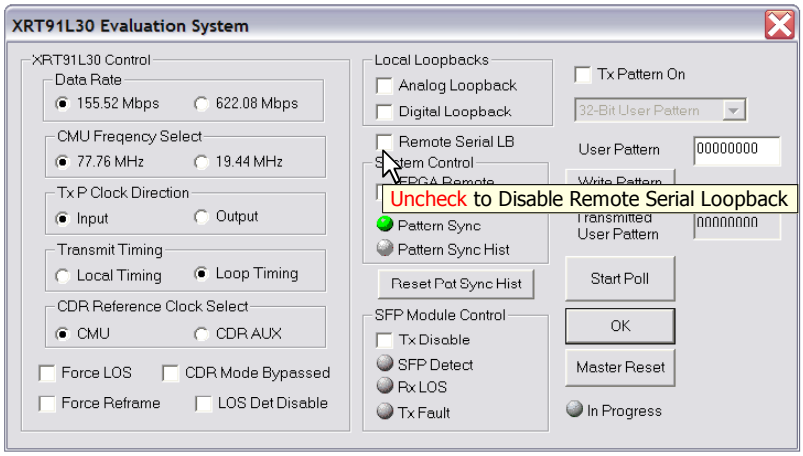



**Step 8.** Check test equipment for valid pattern synchronization.

**Note:** If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and verify data integrity.

**Step 9. (OPTIONAL)** To disable Remote Serial Loopback, uncheck the “Remote Serial LB” box.

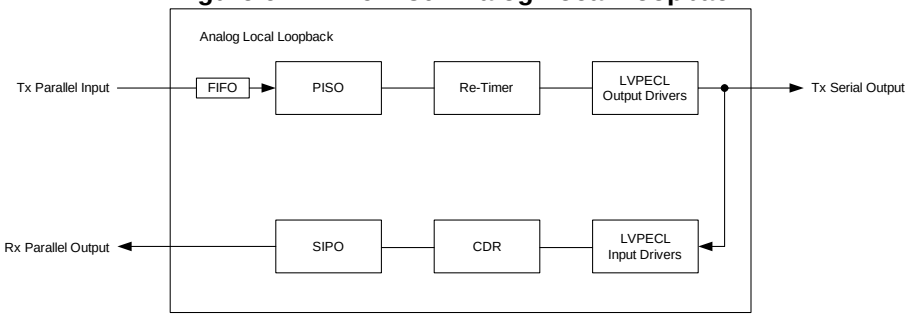
**Figure 6.6 Disable Serial Remote Loopback**



### 6.1.2 PRBS Pattern Synch Test using Analog Local Loopback

This loopback needs to be invoked whenever local diagnostic is desired as such when the PRBS generator and analyzer are used. Local transmit data is looped-back at the analog drivers.

**Figure 6.7 XRT91L30 Analog Local Loopback**

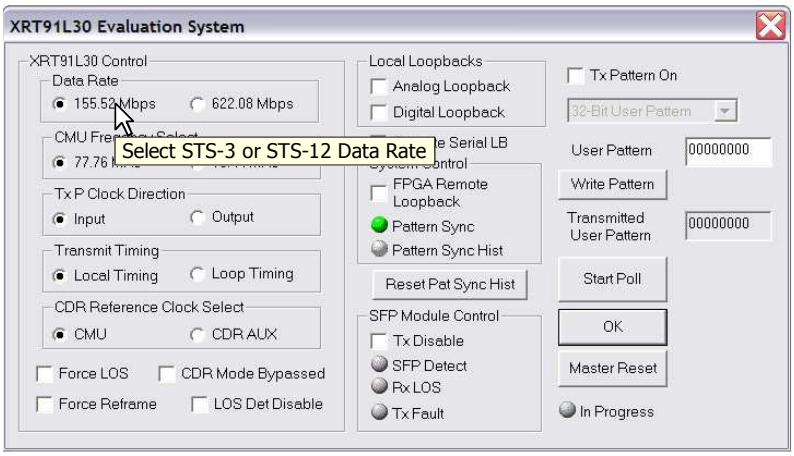



**Configuring for $2^{31}$ – 1 PRBS pattern test using Analog Local Loopback Operation**

**Step 1.** Proceed with the same steps as Step 1 through Step 4 for Remote Serial Loopback Operation in configuring the XRT91L30 board.

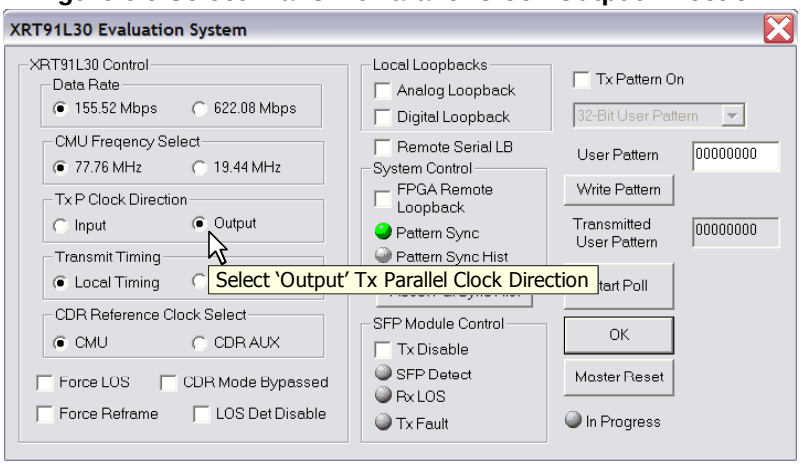
**Step 2.** Select the desired Data Rate signal:
STS-3/STM-1 at 155.52 Mbps or STS-12/STM-4 at 622.08 Mbps

**Figure 6.8 Select Data Rate**



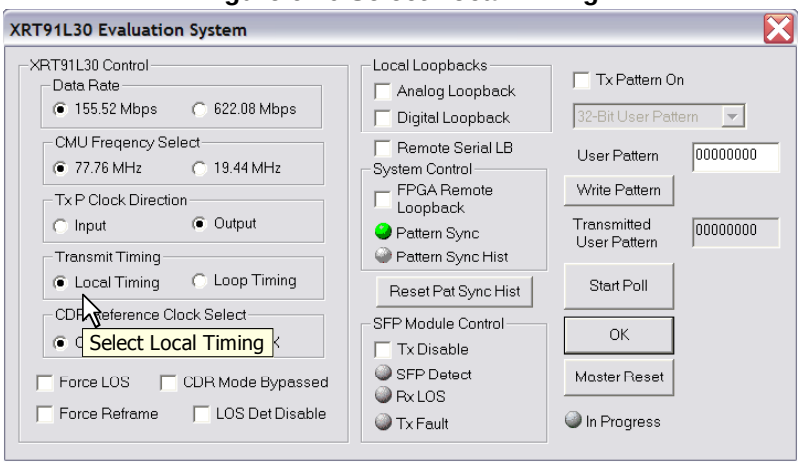
**Step 3.** Select **Output** direction for the XRT91L30 transmit parallel clock. This is due to the FPGA design limitation when using the $2^{31}$ -1 PRBS pattern generator.

**Figure 6.9 Select Transmit Parallel Clock Output Direction**



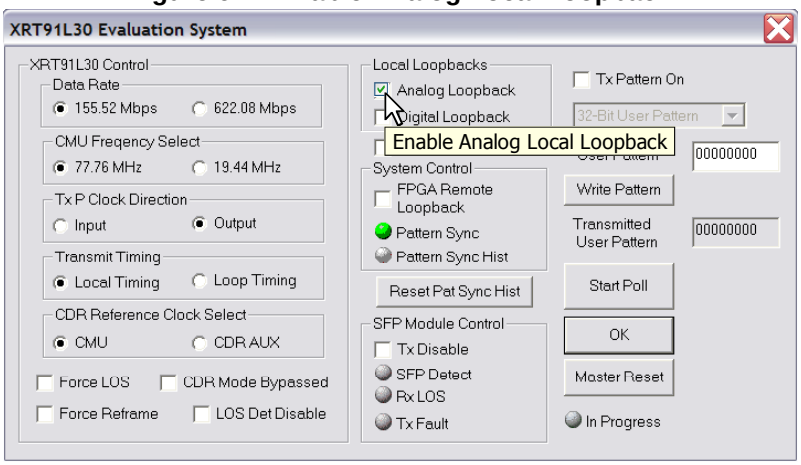

**Step 4.** Select **Local Timing** mode for the XRT91L30 transmit timing.

**Figure 6.10 Select Local Timing**



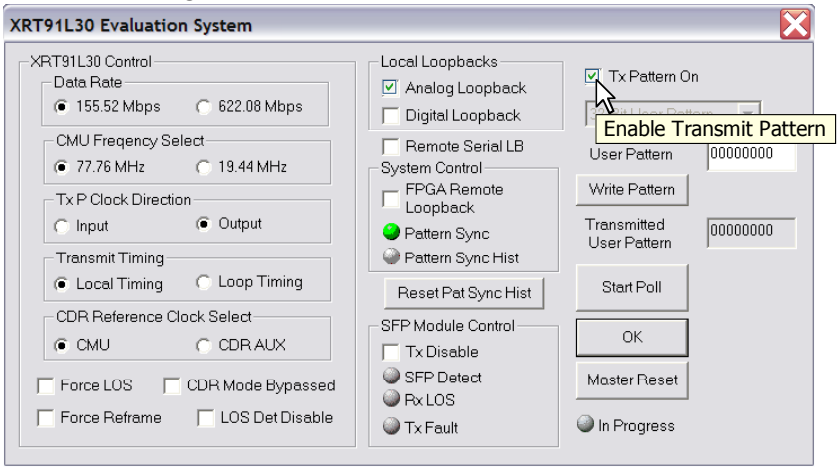
**Step 5.** Enable the Analog Local Loopback by checking the “Analog Loopback” box in **Local Loopbacks** section.

**Figure 6.11 Enable Analog Local Loopback**



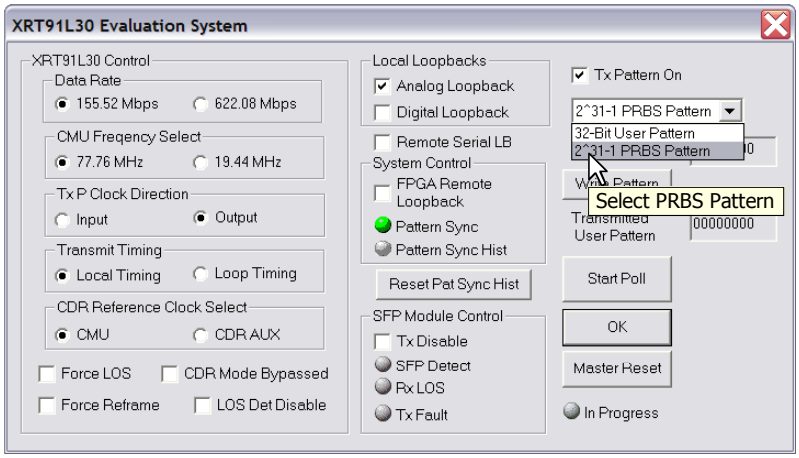

**Step 6.** To enable the transmission of pattern signal from the FPGA, check the “**Tx Pattern On**” box.

**Figure 6.12 Enable Transmit Pattern On**



**Step 7.** To enable the $2^{31}$ -1 PRBS pattern generator and analyzer block within the FPGA, select the "**$2^{31}$ – 1 PRBS Pattern**" box from the pattern selection menu.

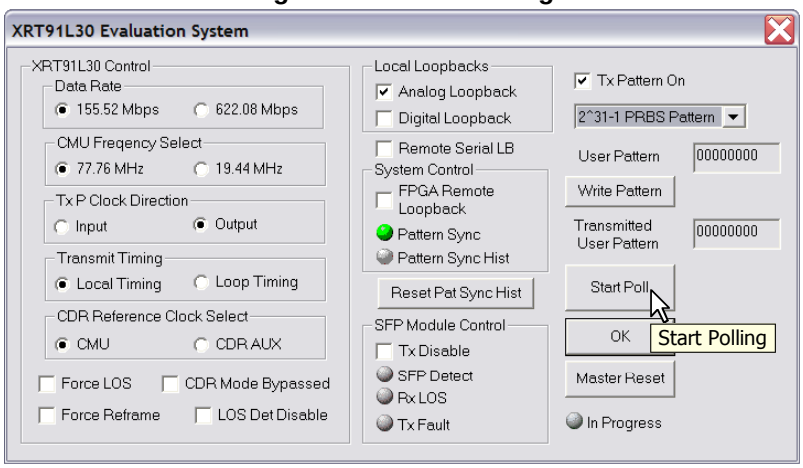
**Figure 6.13 Select $2^{31}$ – 1 PRBS Pattern Generator and Analyzer**




**Note:**
If PRBS Pattern generator and analyzer is not selected ("**32-bit User Pattern**" selected), a 32-bit user pattern defined in the **User Pattern** buffer will be transmitted in lieu of PRBS pattern when "**Tx Pattern On**" is enabled. However, pattern error checking is not available for fixed patterns. The user will not be able to rely on "**Pattern Sync**" and "**Pattern Sync Hist**" for error checking.

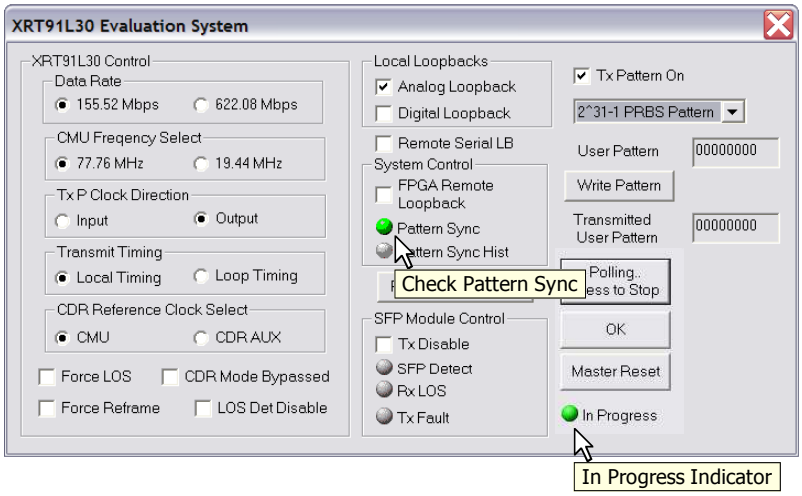
**Step 8.** Check "**Pattern Sync**" status indicator by clicking on "**Start Poll**" button. The "**In Progress**" indicator will start flashing green when polling has begun.

**Figure 6.14 Start Polling**



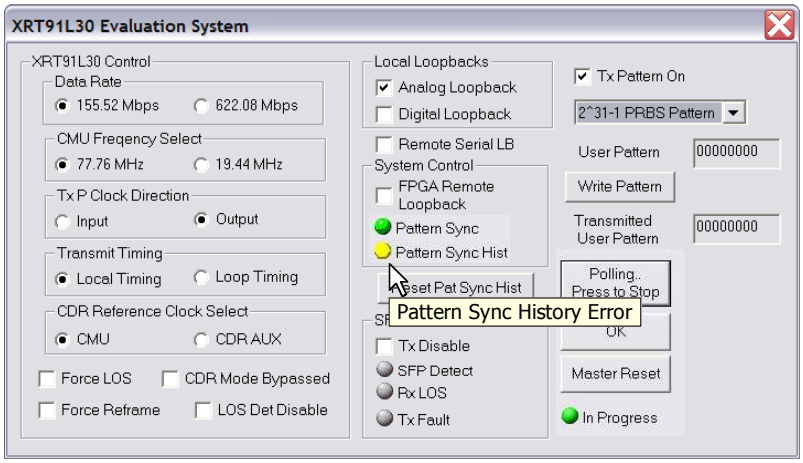
Valid PRBS pattern synchronization is indicated by a green LED. PRBS pattern reception failure is indicated by a red LED.

**Figure 6.15 Check Pattern Sync**



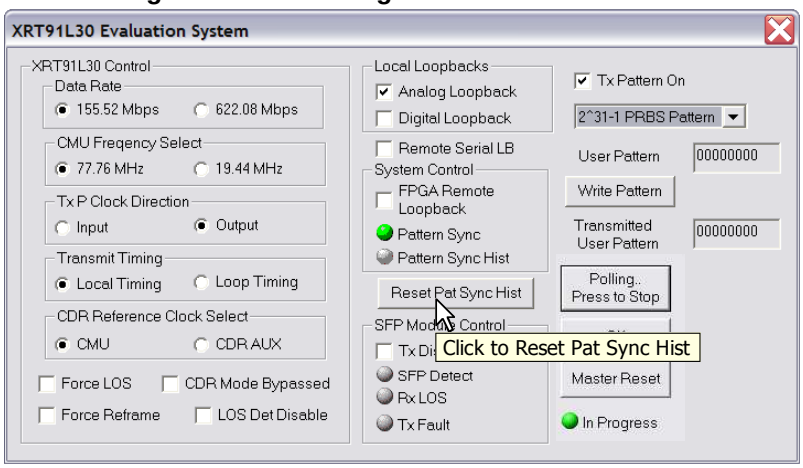

The "**Pattern Sync Hist**" indicator flags momentary errors in PRBS transmission and reception. Momentary and current error occurrence is indicated by a yellow LED.

**Figure 6.16 Check Pattern Loss**



To reset the momentary "**Pattern Sync Hist**" indicator, click the "**Reset Pat Sync Hist**" button.

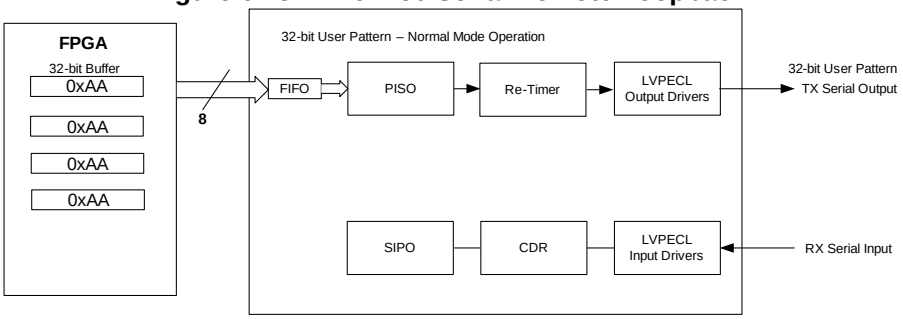
**Figure 6.17 Resetting Pattern Loss Indicator**



## 6.2 TRANSMITTING A USER DESIRED 32-BIT PATTERN

A 32-bit User Pattern can be quickly generated at the FPGA to be transmitted thru the transmit byte-wide parallel interface of XRT91L30.

**Figure 6.18 XRT91L30 Serial Remote Loopback**




**Configuring the XRT91L30 for 32-bit User Pattern Transmission**

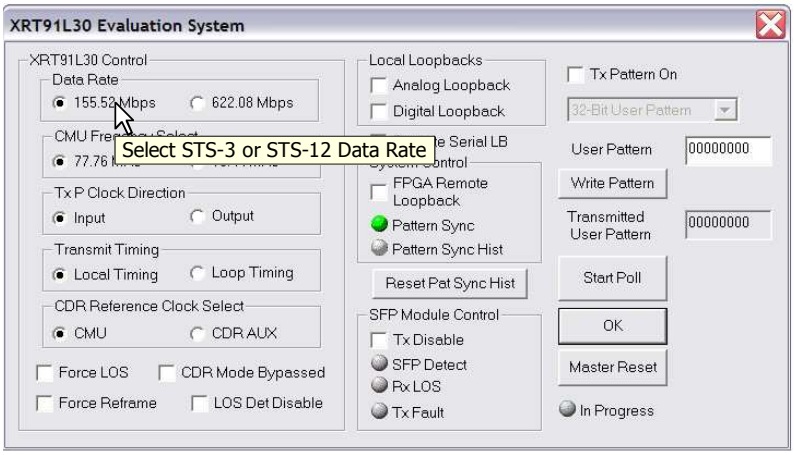
**Step 1.** With the Exar USB drivers and the XRT91L30 GUI installed, connect the USB cable to both the PC and the XRT91L30 Evaluation Board. Verify power supply on the board by checking Power LED.

**Step 2.** Connect the optical cable from the test equipment optical interface to the SFP optical module on the Evaluation Board. This cable is included in the XRT91L30 evaluation kit.

**Step 3.** Launch the XRT91L30 application GUI. See section 4.1, “Starting the Evaluation Software.”

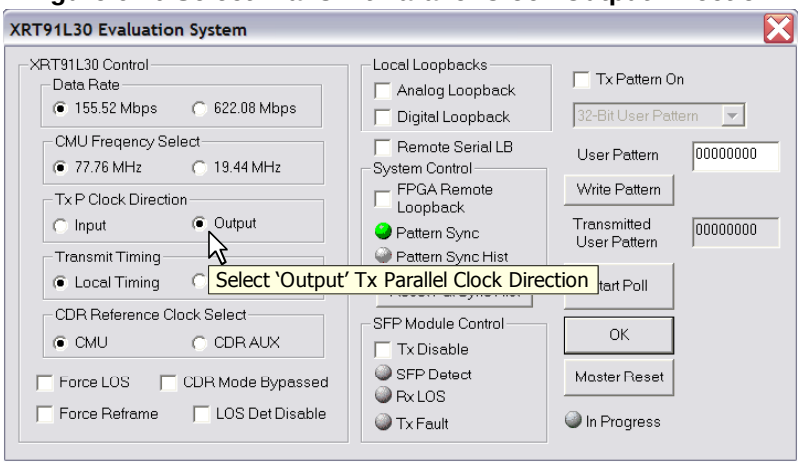
**Step 4.** Once the application GUI **Start Test** is running, select the desired Data Rate signal: STS-3/STM-1 at 155.52 Mbps or STS-12/STM-4 at 622.08 Mbps

**Figure 6.19 Select Data Rate**



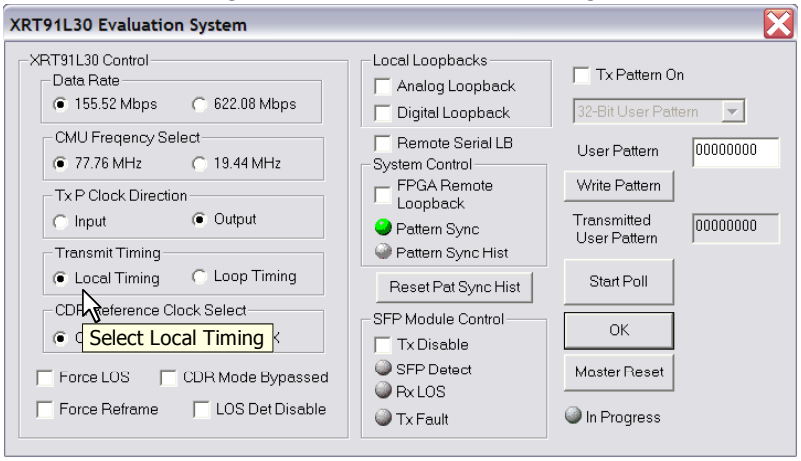
**Step 5.** Select **Output** direction for the XRT91L30 transmit parallel clock. This is due to the FPGA design limitation when using the 32-bit User Pattern generator.

**Figure 6.20 Select Transmit Parallel Clock Output Direction**



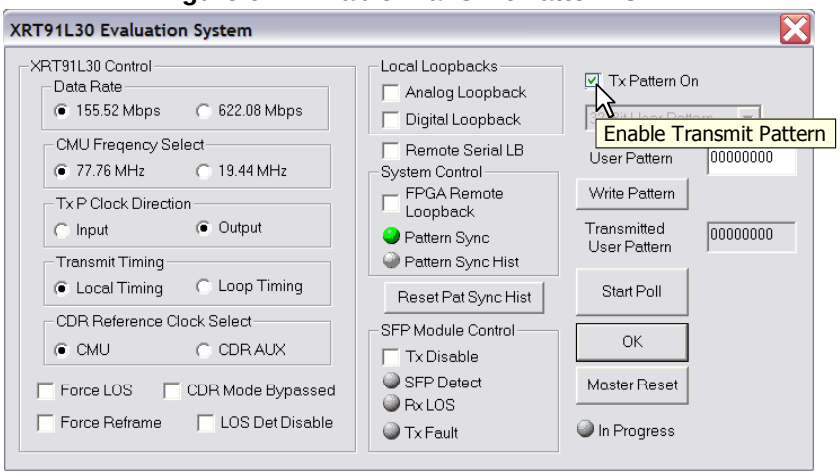

**Step 6.** Select **Local Timing** mode for the XRT91L30 transmit timing.

**Figure 6.21 Select Local Timing**



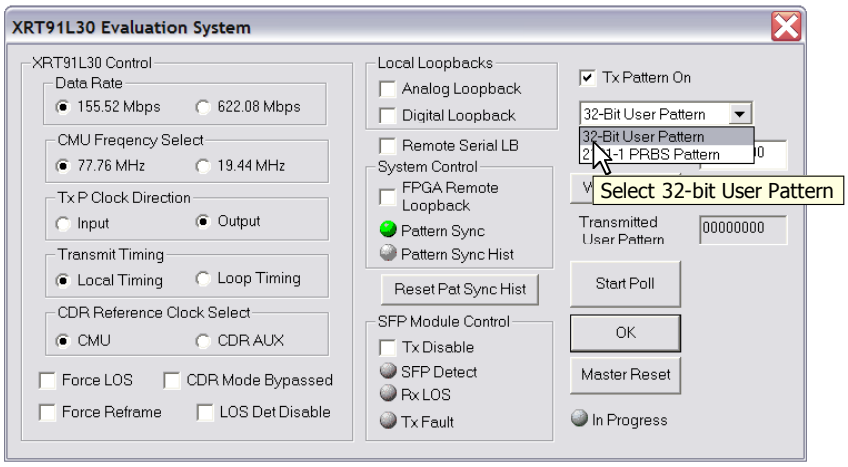
**Step 7.** To enable the transmission of pattern signal from the FPGA, check the "**Tx Pattern On**" box.

**Figure 6.22 Enable Transmit Pattern On**



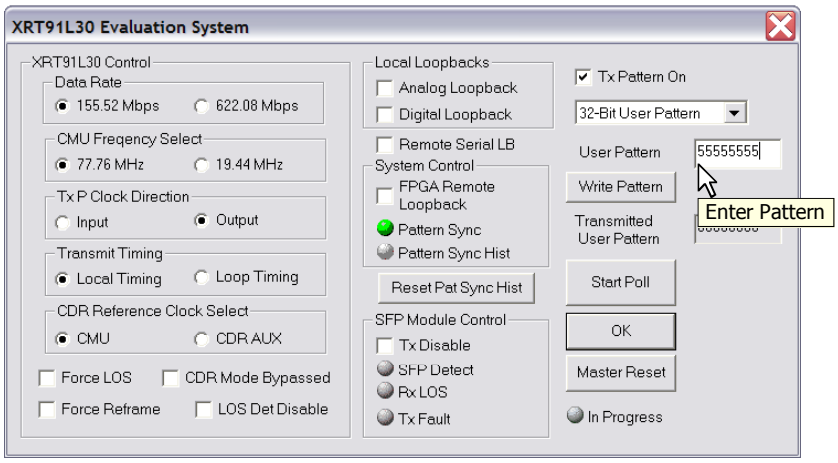

**Step 8.** Select **32-bit User Pattern** on the **Pattern Selection** box below.

**Figure 6.23 Select 32-bit User Pattern**



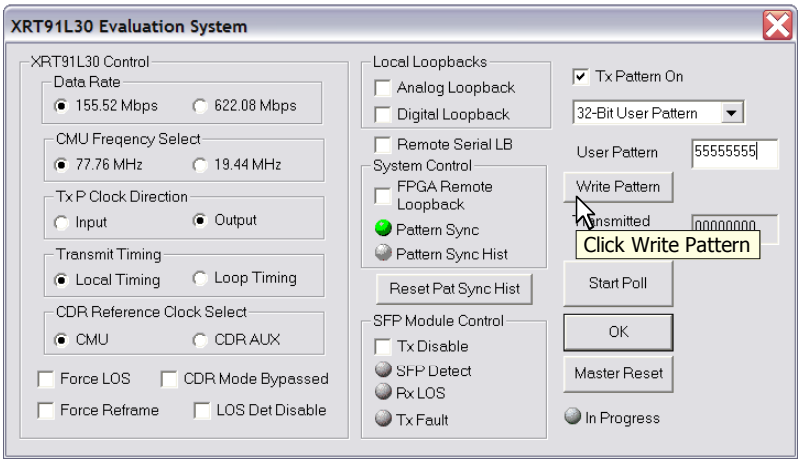
**Step 9.** Enter the value 0xAAAAAAAA to transmit '1010' or 0x55555555 to transmit '0101' pattern.

**Figure 6.24 Enter 32-bit User Pattern**



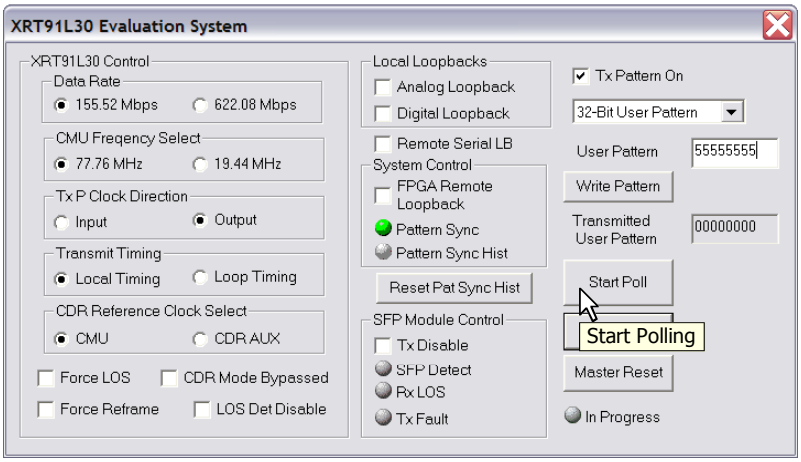

**Step 10.** Click on "**Write Pattern**" to load the user pattern into the FPGA buffer.

**Figure 6.25 Click 'Write Pattern'**



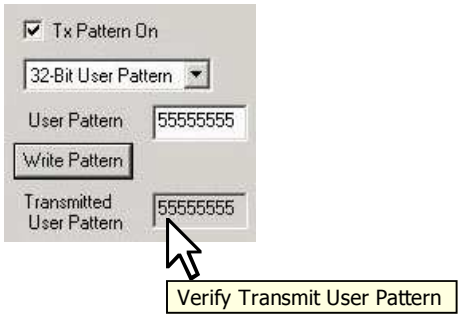
**Step 11.** Click on "**Start Poll**" button. The "**In Progress**" indicator will start flashing green when polling has begun.

**Figure 6.26 Start Polling**




**Step 12.** Verify that the desired pattern is displayed on the "**Transmitted User Pattern**" window. This is the pattern currently transmitted by the XRT91L30.

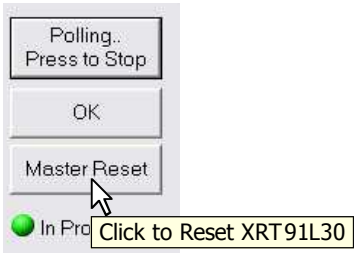
**Figure 6.27 Verify Transmitted Pattern**



### 6.3 MASTER RESET

Whenever necessary, the XRT91L30 can be reset. To invoke this, click on the Master Reset button. This will automatically toggle the hardware reset pin on the XRT91L30.

**Figure 6.28 Master Reset**



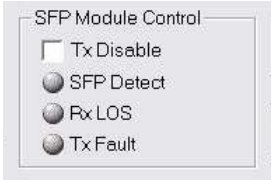

### 6.4 SFP MODULE CONTROL

This section is mainly a register status box that includes the ability to disable the SFP module optical transmitter.

**Table 2.0 SFP Module Control Box**

| | Function | Description |
|---|---|---|
| | Tx Disable | Checking this box disables the optical transmitter |
| | SFP Detect | Red LED detects the absence of the SFP optical module |
| | RxLOS | Red LED detects Loss of Signal |
| | Tx Fault | Red LED detects failure in optical transmission |

**Figure 6.29 SFP Module Control**



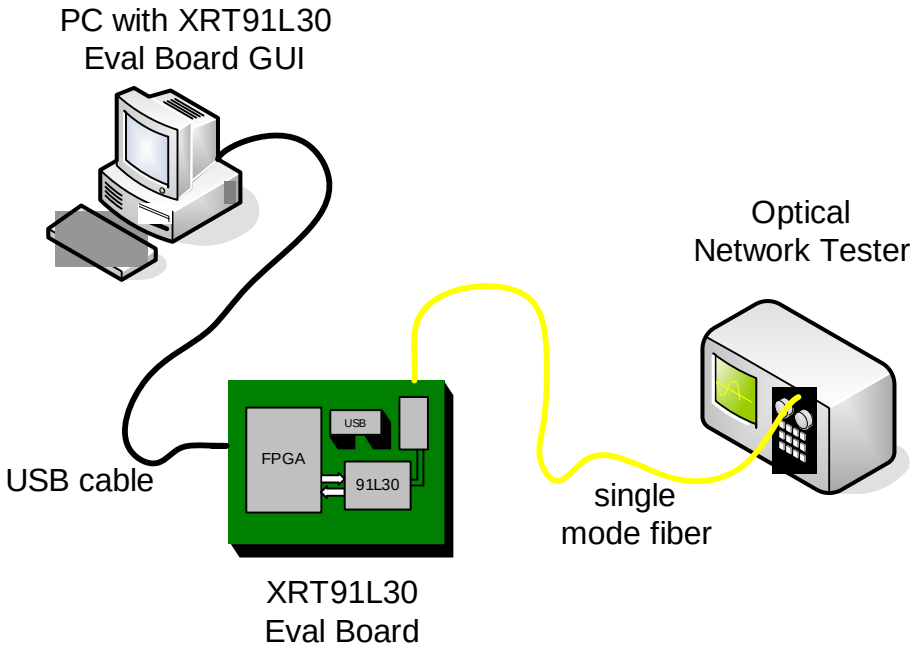
## 7.0 CONFIGURING THE XRT91L30 EVALUATION BOARD FOR JITTER MEASUREMENTS

There are three types of jitter measurement of interest in the XRT91L30 transceiver product. They are received jitter tolerance, jitter transfer, and transmit intrinsic jitter.

- How to measure optical Jitter Tolerance of the XRT91L30
- How to measure optical Jitter Transfer of the XRT91L30
- How to measure optical Intrinsic Jitter of the XRT91L30

Since the XRT91L30 Evaluation Board uses an optical interface, a network tester with an optical interface capable of jitter measurements will be required to successfully characterize optical jitter performance on the XRT91L30. Below is a simple diagram of the jitter measurement setup.

**Figure 7.0 Jitter Measurement Setup**




### 7.1 HOW TO MEASURE OPTICAL JITTER TOLERANCE OF THE XRT91L30

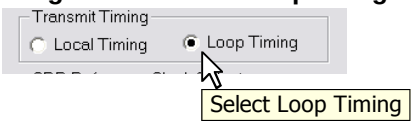
To successfully perform this test, the user needs to configure the XRT91L30 into:

- Remote Serial Loopback
- Looptiming

**Step 1.** Configure the XRT91L30 for Serial Remote Loopback as outlined in the Example Applications in section 6.1.1, Serial Remote Loopback.

**Step 2.** Select **Looptiming** Mode for the XRT91L30 transmit timing.

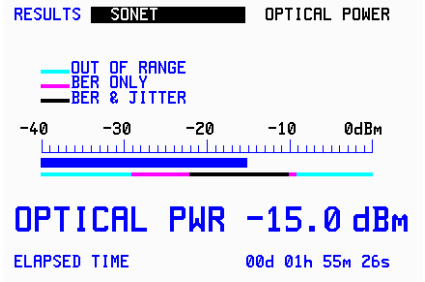
**Figure 7.1 Select Looptiming**




**Step 3.** Select the proper SONET/SDH data rate source and payload pattern on test equipment and verify recovered data integrity and pattern sync on test equipment.

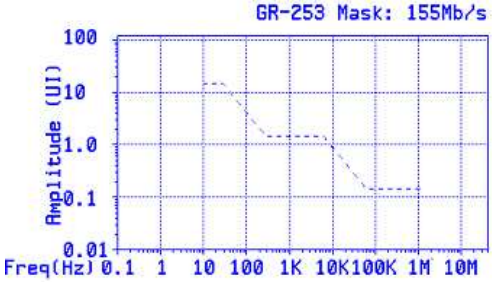
**Step 4.** Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler/connector until desired optical signal strength is achieved for valid jitter measurements.

**Figure 7.2 Optical Signal Strength (Test Equipment)**




**Step 5.** Configure the test equipment for Jitter Tolerance measurements and select the appropriate Jitter Tolerance Mask Standard for SONET STS-12/STS-3 or SDH STM-4/STM-1.

**Figure 7.3 STS-3 GR.253 Jitter Tolerance Mask (Test Equipment)**




**Step 6.** Begin Jitter Tolerance Measurements.

### 7.2 How to measure Optical Jitter Transfer of the XRT91L30

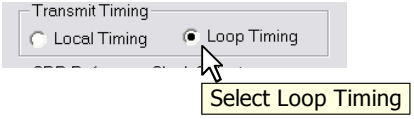
To successfully perform this test, the user needs to configure the XRT91L30 into:

- Remote Serial Loopback
- Looptiming

**Step 1.** Configure the XRT91L30 for Serial Remote Loopback as outlined in the Example Applications in section 6.1.1, Serial Remote Loopback.

**Step 2.** Select **Looptiming** Mode for the XRT91L30 transmit timing.

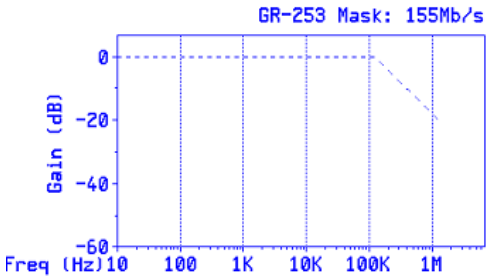
**Figure 7.4 Select Looptiming**




**Step 3.** Select the proper SONET/SDH data rate source and payload pattern on test equipment and verify recovered data integrity and pattern sync on test equipment.

**Step 4.** Configure the test equipment for Jitter Transfer measurements and select the appropriate Jitter Transfer Mask Standard for SONET STS-12/STS-3 or SDH STM-4/STM-1.

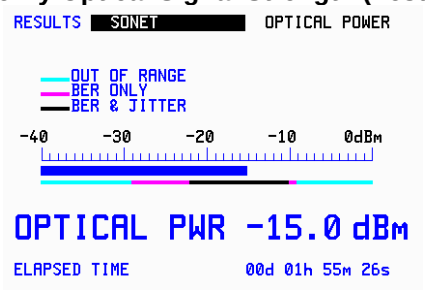
**Figure 7.5 STS-3 GR.253 Jitter Transfer Mask (Test Equipment)**




**Step 5.** Most test equipment will require an initial jitter transfer calibration before proceeding with jitter transfer measurements. Therefore, detach the Evaluation Board connected optical cable from the test equipment and replace a with an optical loopback cable for the calibration process. (See Figure 7.7) Once optical loopback cable is inserted, verify data integrity and pattern sync.

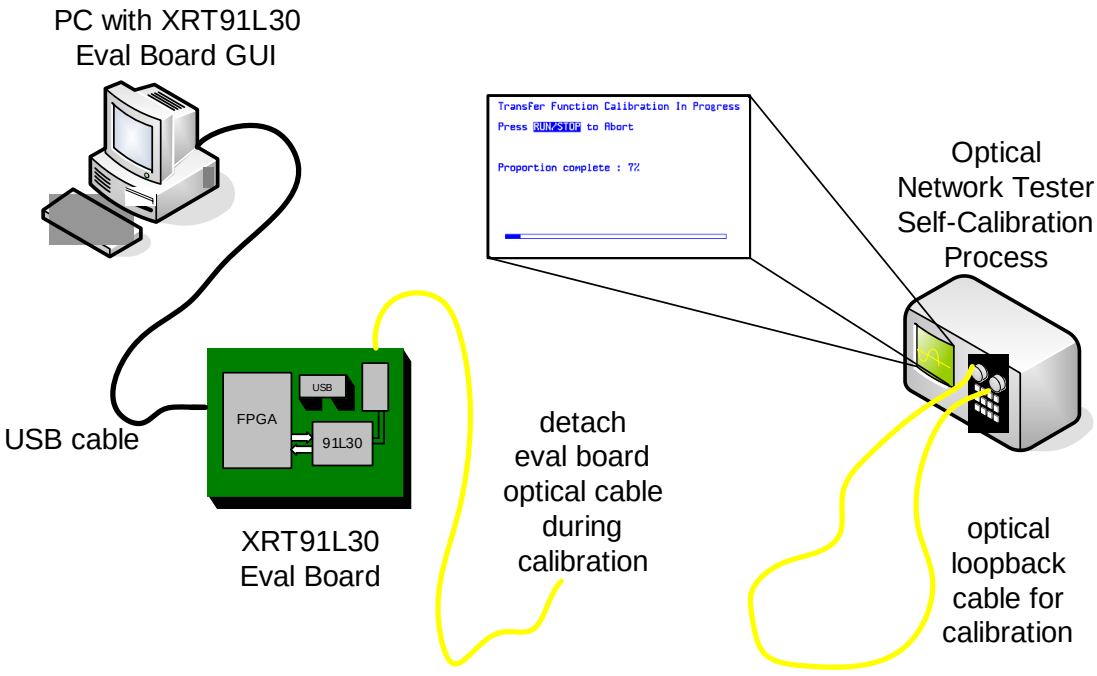
**Step 6**. Verify that the optical signal strength is valid for jitter measurements before proceeding with calibration. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler/connector until desired optical signal strength is achieved for valid jitter measurements.

**Figure 7.6 Verify Optical Signal Strength (Test Equipment)**




**Step 7**. Follow test equipment instructions for calibration and do not interrupt calibration process.

**Figure 7.7 Jitter Transfer Calibration (Test Equipment)**



**Step 8.** Once initial calibration is done, replace the optical loopback cable on the test equipment with the Evaluation Board optical cable. Verify that transmit and receive cables are properly oriented and test equipment receiver does not declare Loss of Signal. Once Evaluation Board optical cable is inserted and data integrity and pattern sync is achieved, verify that the optical signal strength is valid for jitter measurements before proceeding to the next step.

**Figure 7.8 Reattach Evaluation Board optical cable**

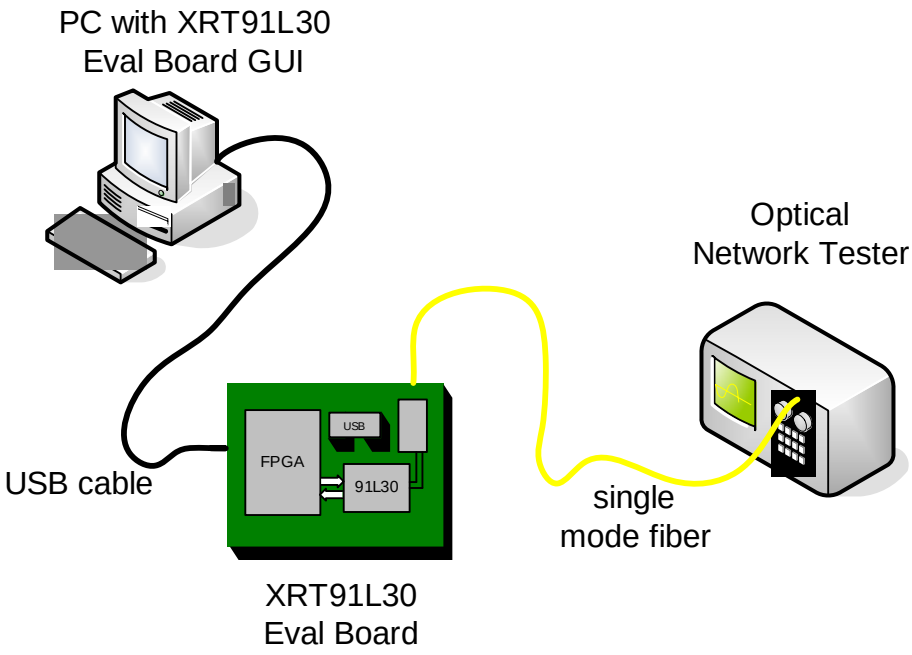
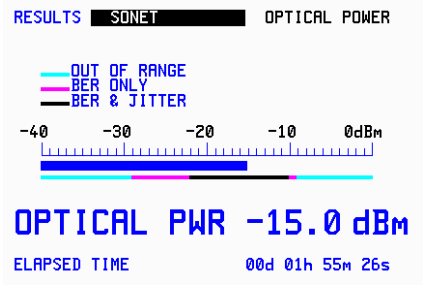



**Figure 7.9 Re-Verify Optical Signal Strength (Test Equipment)**




**Step 9.** Begin Jitter Transfer Measurements.

### 7.3 How to measure Optical Intrinsic Jitter of the XRT91L30

To successfully perform this test, the user needs to configure the XRT91L30 into:

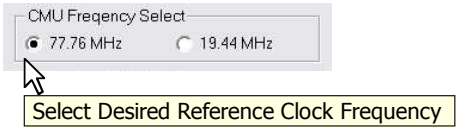
- Transmit a $2^{31}$ -1 PRBS pattern
- Local Timing Mode

**Step 1.** Configure the XRT91L30 to transmit the internally generated $2^{31}$ -1 PRBS pattern as outlined in Example Applications in section 6.1.2, PRBS Pattern Synch Test using Analog Local Loopback. Use step 1 thru step 8.

**Step 2.** Remove the Analog Local Loopback. Do not enable any loopbacks.

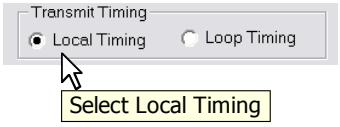
**Step 3.** Select the desired reference clock frequency (77.76 MHz or 19.44 MHz) to be tested.

**Figure 7.10 Select Desired Reference Clock Frequency to be tested**




**Step 4.** Select Local Timing Mode for the XRT91L30 transmit timing.

**Figure 7.11 Select Local Timing**

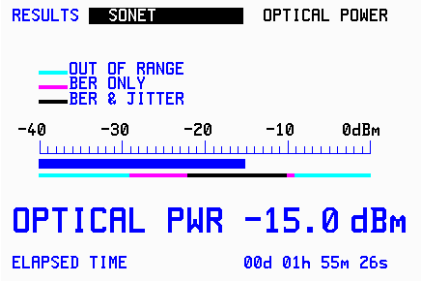



**Step 5.** Select the proper SONET/SDH data rate source on test equipment and verify test equipment is able to obtain valid signal from the XRT91L30 optical transmitter.

**Note:** Since the XRT91L30 is independently transmitting **unframed $2^{31}$ -1 PRBS** pattern to the test equipment, data integrity and pattern sync on the tester is **not** expected. However, tester should detect an unframed OC12/STM-4 or OC3/STM-1 signal.

**Step 5.** Verify that the optical signal strength is valid for jitter measurements. Adjust optical signal strength by adding/removing optical attenuators or slightly adjusting optical coupler until desired optical signal strength is achieved for valid jitter measurements.

**Figure 7.12 Verify Optical Signal Strength (Test Equipment)**




**Step 6.** Configure the test equipment for jitter measurements and select the appropriate SONET/SDH STS-12/STM-4 or STS-3/STM-1 jitter frequency filters on the test equipment according to the table below.

**Table 3.0 SONET/SDH Jitter Frequency Bandpass Filters (1.544 kb/s Networks)**

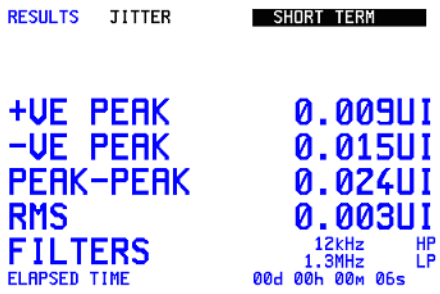
| DATA RATE | SONET GR.253 FILTER STANDARD | SDH G.783 FILTER STANDARD |
|---|---|---|
| 155.52 Mbps | 12 KHz – 1.3 MHz | 12 KHz – 1.3 MHz |
| 622.08 Mbps | 12 KHz – 5.0 MHz | 12 KHz – 5.0 MHz |

**Table 3.1 SONET/SDH Jitter Frequency Bandpass Filters (2048 kb/s Networks)**

| DATA RATE | SONET GR.253 FILTER STANDARD | SDH G.783 FILTER STANDARD |
|---|---|---|
| 155.52 Mbps | 12 KHz – 1.3 MHz | 65 KHz – 1.3 MHz |
| 622.08 Mbps | 12 KHz – 5.0 MHz | 250 KHz – 5.0 MHz |

**Step 7.** Begin measuring jitter and permit test equipment to measure peak-to-peak and rms values over a sixty-second interval (1 minute maximum) per G.783 section 9.3.1.1.

**Figure 7.13 RMS Jitter Measurement (Test Equipment)**



## 8.0 Other Measurements

The following test measurements may also be done on the XRT91L30 Evaluation Board. These types of test may require hardware board modifications.

8.1 Eye diagram test setup
8.2 XRT91L30 Current Consumption Measurement

### 8.1 EYE DIAGRAM TEST SETUP

To display the eye diagram pattern successfully, the user must have the following:

- A high speed digital oscilloscope
- A high impedance or 50 Ohm effective termination differential high speed probe with a minimum bandwidth at least twice the data rate frequency (Use a probe with a minimum of 2 GHz bandwidth)
- The XRT91L30 Evaluation Board schematic for reference.

In addition, the user must configure the XRT91L30 to do the following:

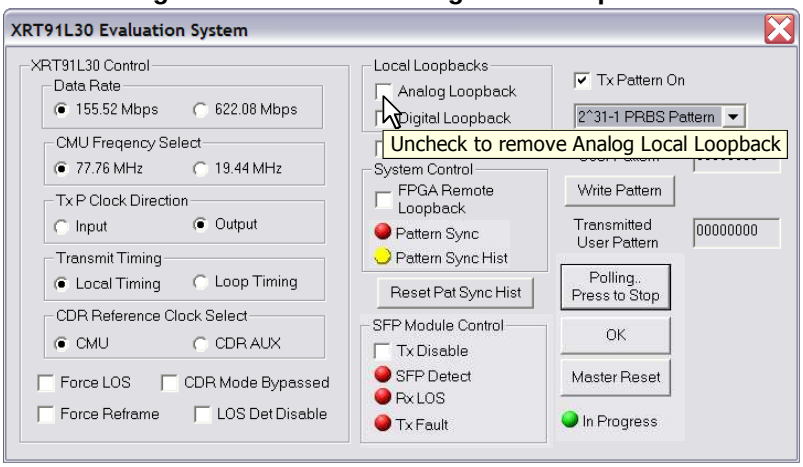
- Transmit $2^{31}$ – 1 PRBS pattern
- Normal Mode of Operation (Remove Loopbacks)
- Local Timing Mode

**Step 1.** Remove the SFP optical module. Find pin 5 and pin 6 of the XRT91L30. These are the TXOP and TXON LVPECL high speed differential outputs, respectively. Prepare the pins for probing, this may or may not require soldering biasing resistors as required by the differential probe manufacturer. Refer to XRT91L30 Evaluation Board schematic for reference and termination information.

**Step 2.** Configure the XRT91L30 to transmit the internally generated $2^{31}$ -1 PRBS pattern as outlined in Example Applications in section 6.1.2, PRBS Pattern Synch Test using Analog Local Loopback. Use step 1 thru step 8.

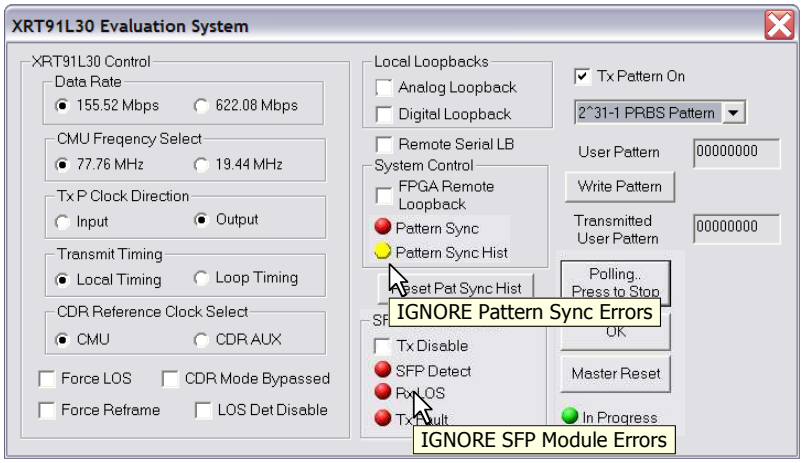
**Step 3.** Remove the Analog Local Loopback. Do not enable any loopbacks.

**Figure 8.0 Remove Analog Local Loopback**



**Step 4. Ignore PRBS Sync** Error and **PRBS Sync Hist** Error. **Ignore SFP Module** errors as well. This error is due to the removal of the SFP optical module and loopbacks being removed and PRBS data not being sent back to the PRBS analyzer.

**Figure 8.1 Ignore PRBS Sync and PRBS Sync Hist Error**

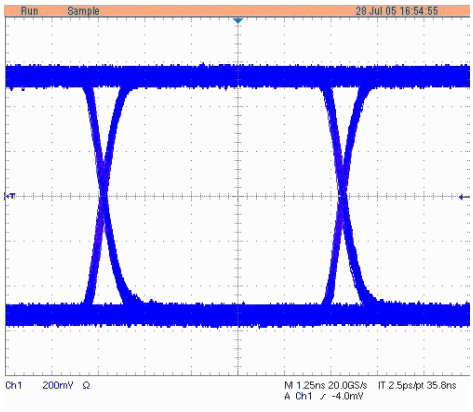



**Step 5.** Securely and gently attach the probe to TXOP and TXON LVPECL high speed differential output pins. Be extremely careful not to subject the pins to physical stress as it may be damaged. Attach the differential probe to the oscilloscope.

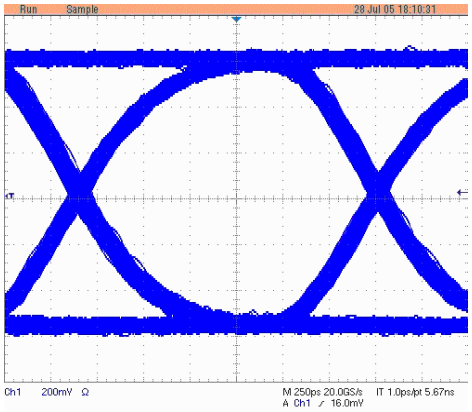
**Step 6.** Configure and adjust the oscilloscope settings to superimpose the XRT91L30 LVPECL high speed differential outputs over time. Your eye diagram should look to something similar below.

**Figure 8.2 XRT91L30 Eye Diagram**

OC-3




OC-12



### 8.2 XRT91L30 CURRENT CONSUMPTION MEASUREMENT

To successfully measure the current consumption on the XRT91L30, the user must have the following:

- A network test equipment capable of sourcing STS-12/STM-4 or STS-3/STM-1.
- A current meter capable of measuring current accurately in milliamps.
- A volt meter capable of measuring voltage accurately in hundredths.
- The XRT91L30 Evaluation Board schematic for reference.

In addition, the user may configure the XRT91L30 to do the following but is not necessary:

- FPGA Remote Loopback
- Looptiming Mode

**Step 1.** Review the XRT91L30 Evaluation Board schematic and locate **L4**. This ferrite bead supplies the entire power to the XRT91L30 silicon. Note that **VccDUT** from the XRT91L30 power supply pins lead to this ferrite bead.

**Step 2.** Locate and remove **L4** ferrite bead on the XRT91L30 Evaluation Board. Store **L4** ferrite bead in a secure container for reinstallation at a later time.

**Step 3.** Attach and secure leads to **L4** soldering pads. It should be long enough to prevent shorting the board. These leads should also be secured and prevented from physical stress when the current meter is attached to the leads. Check for soldering for shorts and remove errant solder on the board before proceeding. The board should be cleaned with a solder flux remover at the soldering site to prevent flux contamination and corrosion.

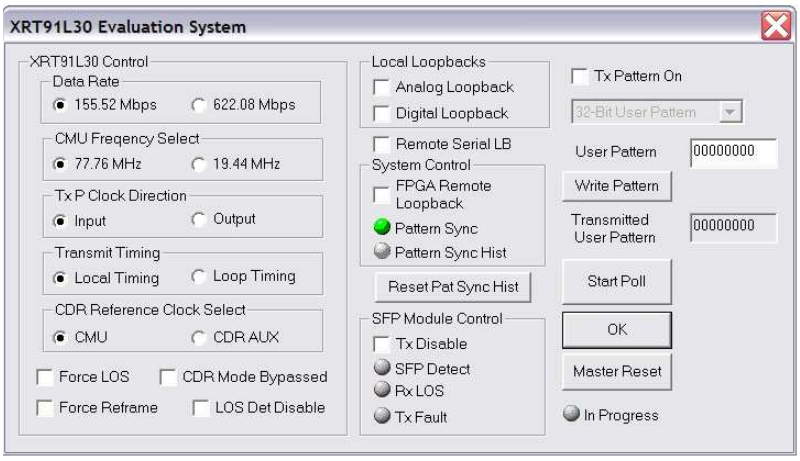
**Step 4.** Connect the USB cable to both the PC and the XRT91L30 Evaluation Board. Verify power supply on the board by checking Power LED. Attach the current meter lead to the **L4 leads** and verify power to the XRT91L30 by monitoring current consumption on the current meter.

**Step 5.** Connect the optical cable from the test equipment optical interface to the SFP optical module on the Evaluation Board. This cable is included in the XRT91L30 evaluation kit.

**Step 6.** Launch the XRT91L30 application GUI. See section 4.1, “Starting the Evaluation Software.”

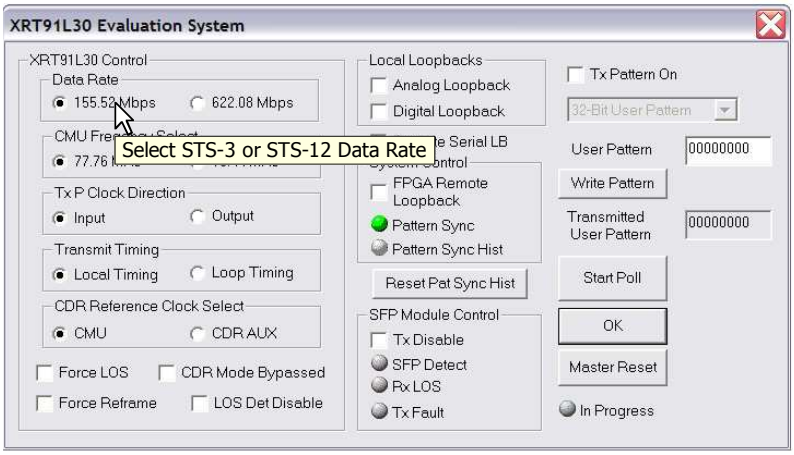
**Step 7.** Once the application GUI **Start Test** is running, you should see a similar window below with the XRT91L30 default settings.

**Figure 8.3 Main GUI Window**



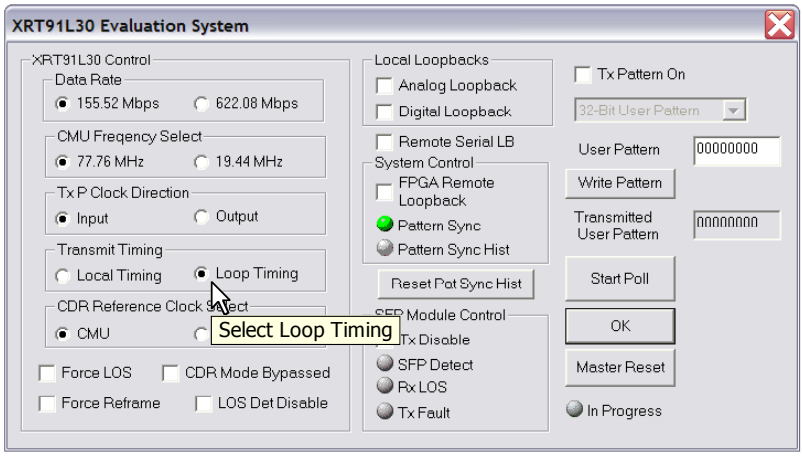

**Step 8.** Select the desired Data Rate signal:
STS-3/STM-1 at 155.52 Mbps or STS-12/STM-4 at 622.08 Mbps

**Figure 8.4 Select Data Rate**



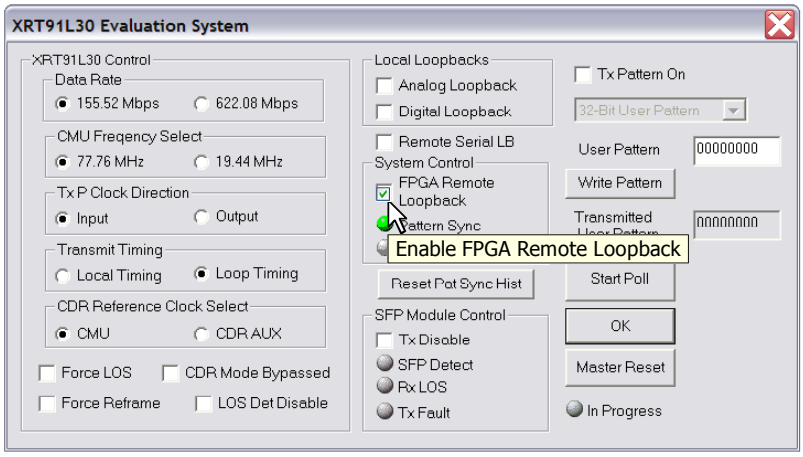
**Step 9.** Select **Looptiming** mode for the XRT91L30 transmit timing.

**Figure 8.5 Select Looptiming**




**Step 10.** Enable the FPGA Remote Loopback by checking the on the "**FPGA Remote Loopback**" box.

**Figure 8.6 Enable FPGA Remote Loopback**




**Step 11.** Check test equipment for valid pattern synchronization.

**Note:** If the test equipment receiver reports a Loss of Signal, it is likely that the optical cable is not properly oriented. Switch the transmit and receive cables on the test equipment and verify data integrity. Check the L4 leads for proper connection as well.

**Step 12.** Record the XRT91L30 current consumption and the voltage at the L4 pad lead with reference to board Ground, the user will need this information to calculate the total power consumption. Note that FPGA Remote Loopback exercises all the logical blocks and analog drivers in the XRT91L30 thereby providing the worst-case condition for power consumption measurement.